Claims

1. A microelectromechanical device comprising at least one thermoelectric layer on a substrate,

wherein a thermal expansion coefficient of said at least one thermoelectric layer differs greatly from a thermal expansion coefficient of the substrate, and

wherein said at least one thermoelectric layer is coupled to at least one stress reduction means for the targeted reduction of lateral mechanical stresses present in the layer.

2. The microelectromechanical device as claimed in claim 1, wherein at least one stress reduction means is arranged between regions of at least one of a functional structure and a region with a thermoelectric layer.

3. The microelectromechanical device as claimed in claim 1, wherein at least one region of the substrate has an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at least one stress reduction means.

4. The microelectromechanical device as claimed in claim 3, wherein the antiadhesion layer comprises at least one of Ti-W alloy and SiO_2.

5. The microelectromechanical device as claimed in claim 1, wherein a vertical offset between two laterally adjoining layers is arranged as said stress reduction means in at least one region on the substrate.

6. The microelectromechanical device as claimed in claim 5, wherein the vertical offset is formed by a prestructuring of the substrateusing at least one of an electrode metal and an adhesion layer.

7. The microelectromechanical device as claimed in claim 1, wherein at least one trench is arranged as said stress reduction means in at least one region of the substrate.

8. The microelectromechanical device as claimed in claim 7, wherein at least one trench has a depth of up to 100 μm.

9. The microelectromechanical device as claimed in claim 1, wherein the difference between the thermal expansion coefficient of at least one layer and the thermal expansion coefficient of the substrate is at least $3 * 10^{-6} K^{-1}$.

10. The microelectromechanical device as claimed in claim 9, wherein the difference between the thermal expansion coefficient of at least one layer and the thermal expansion coefficient of the substrate is at least $10^{-5} K^{-1}$.

11. The microelectromechanical device as claimed in claim 1, wherein the layer thickness of said thermoelectric layer is in the range of 2 and 100 μm.

12. The microelectromechanical device as claimed in claim 11, wherein the layer thickness is in the range of 20 and 100 μm.

13. The microelectromechanical device as claimed in claim 1, wherein the substratecomprises at least one of mica, glass, BaF_2, silicon, silicon dioxide, silicon carbide and diamond.

14. The microelectromechanical device as claimed in claim 1, wherein said thermoelectric layer forms at least one of a Peltier element and a thermogenerator element.

15. The microelectromechanical device as claimed in claim 1, wherein the thermoelectric layer comprises a thermoelectric materialincluding at least one of Bi_2Te_3, PbTe, SiGe and skutterrudite.

16. A method for producing a thermoelectric semiconductor component, the method comprising
forming a layer on a substrate such that the layer is coupled to at least one stress reduction means for the targeted reduction of lateral mechanical stresses present in the layer.

17. The method as claimed in claim 16, wherein forming the layer comprises forming a thermoelectric layer, and wherein the method further comprises arranging said at least one stress reduction means between regions of at least one of a functional structure and a region with a thermoelectric layer.

18. The method as claimed in claim 16, further comprising forming an antiadhesion layer for reducing or preventing the adhesion of material of the layer and thus for forming at

least one stress reduction means in at least one region of the substrate.

19. The method as claimed in claim 16, further comprising arranging a vertical offset between two laterally adjoining layers as said stress reduction means in at least one region on the substrate.

20. The method as claimed in claim 16, further comprising producing at least one trench using at least one of mechanical and chemical processes as said stress reduction means in at least one region of the substrate.

21. A microelectromechanical device comprising:

a substrate having a first thermal expansion coefficient; and

a thermoelectric layer formed over the substrate, the thermoelectric layer having a second thermal expansion coefficient that differs from the first thermal expansion coefficient by at least 10^{-5} K^{-1};

wherein said at least one thermoelectric layer is divided into a plurality of thermoelectric layer portions, each thermoelectric layer portion being separated from adjacent thermoelectric layer portions by a stress reduction region, and

wherein said each thermoelectric layer portion has a thickness in the range of 2 and 100 μm, and an width in the range of 1.4 to 20 mm.